APPENDIX A

(CLEAN VERSION OF SUBSTITUTE SPECIFICATION EXCLUDING CLAIMS)

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APPLICATION FOR LETTERS PATENT

for

METHOD FOR ENCAPSULATING INTERMEDIATE CONDUCTIVE ELEMENTS CONNECTING A SEMICONDUCTOR DIE TO A SUBSTRATE AND SEMICONDUCTOR DEVICES SO PACKAGED

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TITLE OF THE INVENTION

METHOD FOR ENCAPSULATING INTERMEDIATE CONDUCTIVE ELEMENTS CONNECTING A SEMICONDUCTOR DIE TO A SUBSTRATE AND SEMICONDUCTOR DEVICES SO PACKAGED

BACKGROUND

[0001] Field of the Invention: The present invention relates generally to methods for packaging an assembly including a semiconductor die and a substrate element, such as an interposer or a carrier substrate and, more specifically, to a method for introducing an encapsulant material over intermediate conductive elements electronically connecting a semiconductor die and a substrate element. Particularly, the method of the present invention includes disposing tape between the semiconductor die and the substrate element, the intermediate conductive elements being located within a slot formed in the tape, and introducing encapsulant material into the slot.

[0002] Background of the Related Art: The dimensions of many different types of state of the art electronic devices are ever decreasing. To reduce the dimensions of electronic devices, the way in which the microprocessors, memory devices, other semiconductor devices, and other electronic componentry of these devices are packaged and assembled with circuit boards must become more compact.

[0003] One approach to reducing the sizes of assemblies of semiconductor devices and circuit boards has been to reduce the profiles of semiconductor devices and other electronic components upon carrier substrates (e.g., circuit boards) by reducing the distances the semiconductor devices or other electronic components protrude from the carrier substrates. Various types of packaging technologies have been developed to facilitate orientation of semiconductor devices upon carrier substrates in this manner.

[0004] "Flip-chip" technology, one example of which is termed controlled collapse chip connection (C-4) technology, is an example of a packaging and assembly technology that results in a semiconductor device being oriented substantially parallel to a carrier substrate, such as a circuit board. In flip-chip technology, the bond pads or contact pads of a semiconductor device are arranged in an array over a major surface of the semiconductor device. Flip-chip techniques are applicable to both bare and packaged semiconductor devices. A packaged flip-chip type

semiconductor device, which, when an array of discrete conductive elements is located over the major surface, is referred to in the art as a "ball grid array" (BGA) package, typically includes a semiconductor die and a substrate, which is typically termed an "interposer".

[0005] When the interposer of a ball grid array package is positioned adjacent the front surface of the semiconductor die thereof, the bond pads of the semiconductor die on one side of the interposer may be electrically connected to corresponding contact areas on a surface of the opposite side of the interposer by way of intermediate conductive elements, such as bond wires, that extend through one or more holes formed in the interposer. The contact areas communicate through conductive traces with corresponding contact pads bearing discrete conductive elements. In this type of flip-chip semiconductor device assembly, the contact pads are located on the same side of the interposer as the contact pads. This type of flip-chip assembly is positioned adjacent a carrier substrate by orienting the interposer with the contact pad-bearing side thereof facing the carrier substrate.

[0006] The contact pads of the interposer are disposed in an array that has a footprint that mirrors an arrangement of corresponding terminals formed on a carrier substrate. Each of the bond (on bare flip-chip semiconductor dice) or contact (on flip-chip packages) pads and its corresponding terminal may be electrically connected to one another by way of a conductive structure in the form of a discrete conductive element, such as a solder ball, that also spaces the interposer some distance away from the carrier substrate. The space between the interposer and the carrier substrate may be left open or filled with a so-called dielectric "underfill" material that provides electrical insulation between the semiconductor device and the carrier substrate and enhances the mechanical connection between the two components.

[0007] In addition, the intermediate conductive elements that connect the bond pads of the semiconductor die to their corresponding contact areas on the substrate may be encapsulated by introducing material into the opening or openings of the interposer from above the contact pad-bearing side thereof. "Glob-top" type encapsulant materials, such as silicones or epoxies, are typically used for this purpose. Typically, glob-top encapsulant materials have a relatively high viscosity so that the material may be applied to a substantially planar surface without being laterally confined over a particular area of that surface. In comparison with lower viscosity

molding materials, such as transfer molding compounds, which are typically used with some structure to laterally confine the molding material over a specific region of an interposer, the height of the resulting glob-top-encapsulated structure may be greater at or near a centerline of the interposer opening than the encapsulant material thickness that would otherwise be required to properly encapsulate the wire bonds or other intermediate conductive elements that extend over regions of the surface of an interposer that are located adjacent a periphery of an opening formed therethrough. As a result, the overall height of a glop-top encapsulating structure may be undesirably high, providing an undesirably thick semiconductor device package.

[0008] Accordingly, there is a need for a method for encapsulating connections between an interposer and semiconductor die of a semiconductor device assembly that facilitates leak-free introduction of encapsulant from the backside of the semiconductor die and a resulting semiconductor device assembly.

SUMMARY OF THE INVENTION

[0009] The present invention includes a semiconductor device assembly packaging method and semiconductor devices packaged in accordance with the method.

[0010] A packaging method incorporating teachings of the present invention includes assembling a semiconductor die with a substrate element, such as an interposer or a carrier substrate, by disposing a two-sided adhesive tape or other substantially planar member with adhesive on at least portions of both surfaces thereof between the active surface of the semiconductor die and the backside of the substrate element. Bond pads of the semiconductor die are exposed through a slot formed in the tape, as well as through an opening formed through the substrate element and aligned with the slot. At least one end and, preferably, both ends of the slot formed through the tape extend beyond an outer periphery of the semiconductor die. It is preferred, however, that neither end of the slot extends beyond an outer periphery of the substrate element with which the semiconductor die is assembled.

[0011] Wire bonds or other suitable intermediate conductive elements (e.g., tape-automated bonds (TABs) or thermocompression bonds) may be formed between the bond pads of the semiconductor die and the corresponding contacts of the substrate element. Of course, these

intermediate conductive elements extend through the slot of the tape and the opening of the substrate element.

[0012] A coverlay, such as a tape or other substantially planar member having a single side thereof coated with adhesive material, may be disposed over the exposed surface of the substrate element opposite the semiconductor die so as to cover the intermediate conductive elements extending through the substrate element. The coverlay preferably substantially seals the outer substrate element side of the opening formed by the slots of the substrate element and the tape. Thus, the intermediate conductive elements are substantially contained by interior lateral edges of the substrate element and the tape, as well as by the semiconductor die and the coverlay, the only exception being that one or both ends of the slot formed through the tape may be exposed beyond the outer periphery of the semiconductor die. The coverlay may also include one or more recessed areas that are configured to receive the intermediate conductive elements without contacting any portion thereof.

[0013] Next, liquid or gel-like encapsulant material is introduced from above, with the coverlay at the bottom of the assembly, into the slot formed through the tape and the aligned opening formed through the substrate element. The encapsulant material is preferably introduced into the slot through an end thereof that is exposed beyond an outer periphery of the semiconductor die. As encapsulant material fills the slot of the tape and the opening of the substrate element, air is displaced in the channel defined between the semiconductor die, the coverlay and the sides of the aligned tape slot and substrate element opening through another, opposite end of the slot, which is also exposed beyond an outer periphery of the semiconductor die.

[0014] Once the encapsulant material within the channel cures or otherwise becomes at least semisolid, the coverlay may be removed from the substrate element, or contact pads on the substrate element may be exposed through the coverlay and discrete conductive elements may be applied thereto or formed thereon. The packaged semiconductor device may then be tested and used, as known in the art.

[0015] Other features and advantages of the present invention will become apparent to those of skill in the art through consideration of the ensuing description, the accompanying drawings, and the appended claims.

BRIEF DESCRIPTION OF THE DRAWINGS

[0016] In the drawings, which illustrate exemplary embodiments for carrying out the invention:

[0017] FIG. 1 is a perspective view of an assembly including a semiconductor die, a two-sided adhesive tape positioned on and secured to an active surface of the semiconductor die with bond pads of the semiconductor die being exposed through a slot in the tape, and a substrate element secured to an opposite side of the tape from the semiconductor die, the slot of the tape and the bond pads of the semiconductor die being exposed through an aligned opening in the substrate element;

[0018] FIG. 1A is an inverted perspective view of the assembly shown in FIG. 1;

[0019] FIG. 2 is a cross-section taken along line 2–2 of FIG. 1, illustrating the bond pads of the semiconductor die, the slot formed through the tape, and the aligned opening in the substrate element through which the bond pads of the semiconductor die are exposed;

[0020] FIG. 3 is a cross-sectional representation of the assembly shown in FIG. 2, depicting the placement of intermediate conductive elements between the bond pads of the semiconductor die and corresponding contact areas or contact pads on the exposed surface of the substrate element;

[0021] FIG. 4 is a cross-sectional representation of the assembly of FIG. 3, illustrating the positioning of a coverlay over at least a portion of an exposed surface of the substrate element to cover and at least partially contain the intermediate conductive elements that extend between the bond pads of the semiconductor die and their corresponding contact areas or pads of the substrate element;

[0022] FIG. 4A is a cross-sectional representation of the assembly in FIG. 3, illustrating the positioning of a variation of a coverlay, which includes a recessed area, over at least a portion

of the exposed surface of the substrate element to cover and at least partially contain the intermediate conductive elements;

[0023] FIG. 4B is a cross-sectional representation of an assembly similar to that depicted in FIG. 3, but including a variation of the substrate element which includes a recessed area around the opening of the substrate element, and also including a coverlay over at least a portion of the exposed surface of the substrate element to cover and at least partially contain the intermediate conductive elements;

[0024] FIG. 5 is an inverted perspective view of the assembly of FIG. 4, schematically depicting the introduction of encapsulant material into the slot formed through the tape and the aligned opening through the substrate element from above with the backside of the semiconductor die facing upward;

[0025] FIG. 6 is a cross-section taken along line 6–6 of FIG. 5, showing the flow of encapsulant material into the slot formed through the tape and the aligned opening through the substrate element and around the intermediate conductive elements therein;

[0026] FIG. 7 is a perspective view of a package resulting from the process depicted in FIGs. 1-6 when the coverlay depicted in FIG. 4 is used;

[0027] FIG. 7A is a perspective view of a package resulting from the process depicted in FIGs. 1-6 when the coverlay depicted in FIG. 4A is used;

[0028] FIG. 7B is a perspective view of a package resulting from the process depicted in FIGs. 1-6 when the substrate element and coverlay depicted in FIG. 4B are used;

[0029] FIG. 8A is a perspective assembly view of a substrate element strip with tape secured to a backside thereof and of semiconductor dice to be assembled with the substrate element strip;

[0030] FIG. 8B is a perspective view of an assembly including each of the elements shown in FIG. 8A; and

[0031] FIG. 8C is a perspective view of the assembly of FIG. 8B, depicting discrete conductive elements being secured to contact pads of the substrate element.

DETAILED DESCRIPTION OF THE INVENTION

[0032] Referring to FIGs. 1, 1A, and 2, an assembly 1 is illustrated that includes a semiconductor die 10, a substrate element 30, and a dielectric tape 20 positioned between semiconductor die 10 and substrate element 30.

[0033] Semiconductor die 10 includes an active surface 11 and an opposite backside 12. Bond pads 14, which facilitate the communication of electrical signals to and from the various integrated circuits of semiconductor die 10, are carried upon active surface 11. While FIG. 1 illustrates bond pads 14 as being arranged substantially linearly along the center of active surface 11 in a pattern that is typically used to assemble a semiconductor die 10 with a leads-over-chip (LOC) type lead frame, methods incorporating teachings of the present invention are equally applicable to packaging semiconductor dice with different bond pad arrangements.

[0034] Tape 20 is a substantially planar member with two surfaces 21 and 22 that are preferably at least partially coated with adhesive material. Tape 20 also includes a slot 24 formed therethrough, which includes two closed ends. Slot 24 is located such that bond pads 14 of semiconductor die 10 are exposed therethrough when tape 20 is properly aligned over and secured to active surface 11 of semiconductor die 10.

[0035] The material from which tape 20 is formed preferably exhibits a similar coefficient of thermal expansion (CTE) to that of the material of semiconductor die 10. For example, a polyimide tape 20 would be useful with a semiconductor die 10 formed on a silicon substrate element. When semiconductor die 10 and tape 20 have substantially similar, or "matched", coefficients of thermal expansion, the likelihood that these elements of a package will be mechanically stressed during thermal cycling occurring in testing or operation of semiconductor die 10 is reduced.

[0036] As shown, substrate element 30 is an interposer with opposed surfaces 31 and 32. The dimensions of surfaces 31 and 32 of substrate element 30 may be substantially the same as the corresponding dimensions of surfaces 21 and 22 of tape 20. An opening 34 formed through substrate element 30 aligns with bond pads 14 of semiconductor die 10 through slot 24 such that bond pads 14 are exposed through opening 34 when substrate element 30 is properly positioned over active surface 11 of semiconductor die 10. Preferably, opening 34 is substantially

the same size and shape as slot 24 of tape 20 and is aligned therewith upon securing tape 20 to a surface 32 of substrate element 30.

[0037] Substrate element 30 also includes contact areas 36 on surface 31 thereof. Each contact area 36 corresponds to a bond pad 14 of semiconductor die 10. In addition, surface 31 of the illustrated substrate element 30 carries contact pads 38, each of which corresponds to a contact area 36 and communicates therewith by way of a conductive element 37 that extends between contact pad 38 and contact area 36.

[0038] The material from which substrate element 30 is formed preferably has a coefficient of thermal expansion that is similar to or substantially the same as those of the materials of tape 20 and semiconductor die 10. For example, a substrate element 30 formed from silicon would have a similar coefficient of thermal expansion to those of a polyimide tape 20 and a silicon semiconductor die 10. Alternatively, other materials that may be used to fabricate flexible or rigid substrate elements, such as ceramics, FR-4 resin, or polyimide, may be used to form substrate element 30.

[0039] While the drawings depict substrate element 30 as being an interposer, the method of the present invention may also be used to package assemblies with other types of substrate elements, including, without limitation, other carrier substrate elements.

[0040] In forming assembly 1, tape 20 may be positioned relative to and secured to both active surface 11 of semiconductor die 10 and surface 32 of substrate element 30. When semiconductor die 10, tape 20, and substrate element 30 are properly positioned relative to one another, bond pads 14 of semiconductor die 10 are exposed through both slot 24 of tape 20 and aligned opening 34 of substrate element 30.

[0041] As shown in FIG. 1A, ends 25 and 26 of slot 24 formed through tape 20 and corresponding ends of opening 34 may extend beyond an outer periphery 15 of semiconductor die 10. Preferably, however, neither end 25, 26 of slot 24 extends beyond an outer periphery 35 of substrate element 30.

[0042] Once semiconductor die 10, tape 20, and substrate element 30 have been properly positioned relative to one another and secured to one another to form assembly 1, each bond pad 14 of semiconductor die 10 may be electrically connected to its corresponding contact

area 36 of substrate element 30. As shown in FIG. 3, this may be done by placing or forming an intermediate conductive element 40, such as the illustrated wire bond or a tape-automated bond (i.e., flex circuit) or thermocompression bond, between each bond pad 14 and its corresponding contact area 36, through slot 24 of tape 20 and opening 34 of substrate element 30, and by bonding respective ends of intermediate conductive element 40 to bond pad 14 and to contact area 36, as known in the art.

[0043] Since slot 24 and opening 34 extend beyond outer periphery 15 of semiconductor die 10, as shown in FIG. 1A, apparatus that form or position intermediate conductive elements 40, such as a wire bonding capillary, may better access bond pads 14 located at or near outer periphery 15.

[0044] Turning now to FIG. 4, a coverlay 42, which may comprise tape or another substantially planar member, one side of which is coated with adhesive material, is positioned on surface 31 of substrate element 30. While coverlay 42 may cover substantially the entire surface 31, coverlay need only substantially cover opening 34 and intermediate conductive elements 40 that extend through opening 34. Coverlay 42 may be aligned with surface 31 by known processes and secured thereto, as known in the art. The adhesive material of coverlay 42 preferably facilitates the ready removal of coverlay 42 from surface 31 once coverlay 42 is no longer needed. By way of example, a pressure sensitive adhesive that will withstand the conditions of subsequent processes may be used on coverlay 42. Coverlay 42 preferably has sufficient flexibility to conform to any irregularities or nonplanarities of surface 31 of substrate element 30, such as the portions of intermediate conductive elements 40 that extend over surface 31 and contact areas 36 located on surface 31.

[0045] Once coverlay 42 has been secured to surface 31 of substrate element 30 and over opening 34 thereof, intermediate conductive elements 40 are at least partially laterally contained within a receptacle formed by coverlay 42, the peripheral edges of opening 34, and the peripheral edges of slot 24 formed through tape 20. At the side of opening 34 opposite tape 20, intermediate conductive elements 40 are contained by coverlay 42. In addition, with the exception of the exposed ends 25, 26 (FIG. 1A) of slot 24 that are located outside the periphery

15 of semiconductor device 10, intermediate conductive elements 40 are also partially contained by semiconductor device 10.

[0046] As depicted in FIG. 4, coverlay 42 includes a single, substantially planar layer of material. Alternatively, as shown in FIG. 4A, a variation of coverlay 42′ includes two layers 42a′ and 42b′, one layer 42a′ of which is substantially continuous, while the other layer 42b′ includes an aperture 43′ therethrough. When layers 42a′ and 42b′ are secured to one another, aperture 43′ forms a recess 44′ within a surface of coverlay 42′. Aperture 43′ and recess 44′ formed thereby are located to receive the portions of intermediate conductive elements 40 that extend over surface 31 of substrate element 30 upon placement of coverlay 42′ on surface 31. Preferably, when coverlay 42′ is secured to surface 31, coverlay 42′ does not contact any portion of intermediate conductive elements 40, thereby subsequently facilitating the substantially complete encapsulation of intermediate conductive elements 40.

[0047] Alternative means by which intermediate conductive elements 40 may be substantially contained and subsequently encapsulated are shown in FIG. 4B, which illustrates a variation of a substrate element 30″ that may be used in methods and semiconductor device packages incorporating teachings of the present invention. A surface 31″ of substrate element 30″ may include a recessed area 33″ which surrounds opening 34″. Recessed area 33″, within which contact areas 36″ are located, is configured to receive the portions of intermediate conductive elements 40 that extend over surface 31″. Accordingly, a substantially planar coverlay 42, such as that described in reference to FIG. 4, may be secured to surface 31″ of substrate element 30″ without substantially contacting intermediate conductive elements 40.

[0048] FIGs. 5 and 6 show assembly 1 in an inverted orientation, with backside 12 of semiconductor die 10 and the exposed ends 25, 26 of slot 24 formed through tape 20 facing upward. Using an encapsulant dispenser needle 50 of a type known in the art, a suitable, known type of dielectric encapsulant material 52 may be introduced into slot 24 of tape 20 and opening 34 of substrate element 30 through an exposed end 25 of slot 24. As encapsulant material 52 is being introduced into slot 24, air within slot 24 is displaced through the other end 26 thereof. In addition to containing encapsulant material 52 within slot 24 and opening 34, coverlay 42 also laterally confines encapsulant material 52 over surface 31 of substrate element 30. Preferably,

when slot 24 and opening 34 are substantially filled with encapsulant material 52, encapsulant material 52 substantially encapsulates intermediate conductive elements 40.

[0049] Once slot 24 and opening 34 are substantially completely filled with encapsulant material 52, encapsulant material 52 may be permitted to harden, if a thermoplastic resin, or known processes may be employed to cure or set other types of encapsulant materials 52 (e.g., by application of heat and/or pressure to thermoset resins, by exposure of photoimageable polymer encapsulant materials to an appropriate wavelength of radiation, or by use of an appropriate catalyst for other types of materials). Together, encapsulant material 52 and tape 20 substantially encapsulate active surface 11 of semiconductor device 10 and fill the gap between active surface 11 and surface 32 of substrate element 30.

[0050] Once encapsulant material 52 has hardened, all or a portion of coverlay 42, 42′ may be removed from substrate element 30, 30″ so as to expose at least contact pads 38, 38′ thereof, as depicted in FIGs. 7, 7A, and 7B, and form an operable semiconductor device package 2, 2′, 2″.

[0051] An alternative method for packaging semiconductor dice 10 in accordance with teachings of the present invention, which involves the use of substrate element strips 3‴, each of which includes a plurality of connected substrate elements 30‴ formed thereon, is shown in FIGs. 8A and 8B.

[0052] As shown in FIG. 8A, each substrate element 30‴ of substrate element strip 3‴ includes an elongate opening 34‴ formed therethrough, as well as contact areas 36‴ positioned on a surface 32‴ of substrate element 30‴, proximate its opening 34‴ and contact pads 38‴ corresponding to and in communication with contact areas 36‴.

[0053] An elongate tape 20‴, which includes a plurality of slots 24‴ formed therethrough, each slot 24‴ corresponding to an opening 34‴ of a substrate element 30‴ of substrate element strip 3‴, may be positioned adjacent and secured to a backside 31‴ of substrate element strip 3‴.

[0054] A semiconductor die 10 may be aligned with each substrate element 30‴ formed on substrate element strip 3‴, as shown in FIG. 8A, and secured to substrate element 30‴ by way of tape 20‴, as illustrated in FIG. 8B. When semiconductor dice 10 are properly positioned,

upon securing semiconductor dice 10 to tape 20‴ and, thus, to substrate element strip 3‴, bond pads 14 on each semiconductor die 10 are exposed through their corresponding slot 24‴ of tape 20‴, as well as through their corresponding opening 34‴ of the corresponding substrate element 30‴.

[0055] In addition, as depicted in FIG. 8C, discrete conductive elements 5 may be formed on or secured to contact pads 38‴ on surface 32‴ of each substrate element 30‴ to facilitate connection of each substrate element 30‴ to a higher level substrate, such as a circuit board, or to another semiconductor device, as known in the art. Discrete conductive elements 5 may comprise, for example, balls, bumps, pillars, columns, or other structures formed from one or more metals (e.g., solder, gold, etc.), conductive epoxies, conductor-filled epoxies, or z-axis conductive elastomers.

[0056] Once each semiconductor die 10 and its corresponding substrate element 30‴ have been electrically connected to each other and packaged, such as by the processes disclosed herein in reference to FIGs. 3-6, adjacent packages may be severed or otherwise separated from one another by known techniques, such as by use of a wafer saw or otherwise, as known in the art.

[0057] In the illustrated embodiments of the inventive semiconductor device package, tape 20 comprises the majority of material between semiconductor die 10 and substrate element 30, while encapsulant material 52 covers a relatively small portion of active surface 11 of semiconductor die 10. If, as is preferred, the coefficient of thermal expansion of tape 20 is substantially the same as or similar enough to the coefficient of thermal expansion of semiconductor die 10, the thermally induced mechanical stresses (i.e., by adjacent, thermally mismatched layers or structures) that will be applied to a package during operation of semiconductor die 10 will be minimized. If substrate element 30 is also formed from silicon or another material having substantially the same or a similar enough coefficient of thermal expansion to that of semiconductor die 10, thermally induced mechanical stresses on package 2, 2′, 2″ will be further minimized.

[0058] Although the foregoing description contains many specifics, these should not be construed as limiting the scope of the present invention, but merely as providing illustrations of

some exemplary embodiments. Similarly, other embodiments of the invention may be devised which do not depart from the spirit or scope of the present invention. Features from different embodiments may be employed in combination. The scope of the invention is, therefore, indicated and limited only by the appended claims and their legal equivalents, rather than by the foregoing description. All additions, deletions, and modifications to the invention, as disclosed herein, which fall within the meaning and scope of the claims are to be embraced thereby.